



**SKYPER™**

## IGBT Driver Core

### SKYPER 32 R

Preliminary Data

### Features

- Two output channels
- Integrated potential free power supply
- Under voltage protection
- Drive interlock top / bottom
- Dynamic short circuit protection
- Shut down input
- Failure management
- IEC 60068-1 (climate) 40/085/56, no condensation and no dripping water permitted, non-corrosive, climate class 3K3 acc. EN60721

### Typical Applications

- Driver for IGBT modules in bridge circuits in choppers, inverter drives, UPS and welding inverters
- DC bus voltage up to 1200 V

- 1) with external high voltage diode
- 2) Please Note: the isolation test is not performed as a series test at SEMIKRON and must be performed by the user
- 3) according to VDE 0110-20
- 4) can be expanded to 6,3μQ with boost capacitors

Isolation coordination in compliance with EN50178 PD2

Operating temperature is real ambient temperature around the driver core

Degree of protection: IP00

### Absolute Maximum Ratings

Symbol	Conditions	Values	Units
$V_S$	Supply voltage primary	16	V
$V_{iH}$	Input signal voltage (High)	$V_S + 0,3$	V
$V_{iL}$	Input signal voltage (Low)	GND - 0,3	V
$I_{outPEAK}$	Output peak current	15	A
$I_{outAVmax}$	Output average current	50	mA
$f_{max}$	Max. switching frequency	50	kHz
$V_{CE}$	Collector emitter voltage sense across the IGBT <sup>1)</sup>	1700	V
dv/dt	Rate of rise and fall of voltage secondary to primary side	50	kV/μs
$V_{isolIO}$	Isolation test voltage input - output (AC, rms, 2s) <sup>2)</sup>	4000	V
$V_{isolPD}$	Partial discharge extinction voltage, rms, $Q_{PD} \leq 10pC$ <sup>3)</sup>	1500	V
$V_{isol12}$	Isolation test voltage output 1 - output 2 (AC, rms, 2s) <sup>2)</sup>	1500	V
$R_{Gonmin}$	Minimum rating for $R_{Gon}$	1,5	Ω
$R_{Goffmin}$	Minimum rating for $R_{Goff}$	1,5	Ω
$Q_{out/pulse}$	Max. rating for output charge per pulse	2,5 <sup>4)</sup>	μC
$T_{op}$	Operating temperature	- 40 ... + 85	°C
$T_{stg}$	Storage temperature	- 40 ... + 85	°C

### Characteristics

$T_a = 25^\circ C$ , unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
$V_S$	Supply voltage primary side	14,4	15	15,6	V
$I_{SO}$	Supply current primary side (no load)	80			mA
	Supply current primary side (max.)			450	mA
$V_i$	Input signal voltage on/off		15 / 0		V
$V_{iT+}$	Input threshold voltage (High)			12,3	V
$V_{iT-}$	Input threshold voltage (Low)	4,6			V
$R_{in}$	Input resistance (switching signals)		10		kΩ
	Internal pull-up resistance shut down input (5V logic)		3,3		kΩ
$V_{G(on)}$	Turn on gate voltage output		+ 15		V
$V_{G(off)}$	Turn off gate voltage output		- 7		V
$f_{ASIC}$	Asic system switching frequency		8		MHz
$t_{d(on)IO}$	Input-output turn-on propagation time		1,1		μs
$t_{d(off)IO}$	Input-output turn-off propagation time		1,1		μs
$t_{d(terr)}$	Error input-output propagation time	5,4		7,9	μs
$t_{pERRRESET}$	Error reset time		9		μs
$t_{TD}$	Top-Bot Interlock Dead Time		3		μs
$C_{ps}$	Coupling capacitance primary secondary		12		pF
w	weight		28		g
MTBF	Mean Time Between Failure @ $T_a = 40^\circ C$ , max. load		2,5		$10^6$ h

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## Technical Explanations

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 Prepared by: Markus Hermwille

*This Technical Explanation is valid for the following parts:*

*Related Documents:*

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# SKYPER™ 32 R

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**Please note:**

Unless otherwise specified, all values in this technical explanation are typical values. Typical values are the average values expected in large quantities and are provided for information purposes only. These values can and do vary in different applications. All operating parameters should be validated by user's technical experts for each application.

## Application and Handling Instructions

- Please provide for static discharge protection during handling. As long as the hybrid driver is not completely assembled, the input terminals have to be short-circuited. Persons working with devices have to wear a grounded bracelet. Any synthetic floor coverings must not be statically chargeable. Even during transportation the input terminals have to be short-circuited using, for example, conductive rubber. Worktables have to be grounded. The same safety requirements apply to MOSFET- and IGBT-modules.
- Any parasitic inductances within the DC-link have to be minimised. Over-voltages may be absorbed by C- or RCD-snubbers between main terminals for PLUS and MINUS of the power module.
- When first operating a newly developed circuit, SEMIKRON recommends to apply low collector voltage and load current in the beginning and to increase these values gradually, observing the turn-off behaviour of the free-wheeling diode and the turn-off voltage spikes generated across the IGBT. An oscillographic control will be necessary. Additionally, the case temperature of the module has to be monitored. When the circuit works correctly under rated operation conditions, short-circuit testing may be done, starting again with low collector voltage.
- It is important to feed any errors back to the control circuit and to switch off the device immediately in failure events. Repeated turn-on of the IGBT into a short circuit with a high frequency may destroy the device.
- The inputs of the hybrid driver are sensitive to over-voltage. Voltages higher than  $V_S + 0,3V$  or below  $-0,3V$  may destroy these inputs. Therefore, control signal over-voltages exceeding the above values have to be avoided.
- The connecting leads between hybrid driver and the power module should be as short as possible (max. 20cm), the driver leads should be twisted.

## Further application support

Latest information is available at <http://www.semikron.com>. For design support please read the SEMIKRON Application Manual Power Modules available at <http://www.semikron.com>.

## General Description

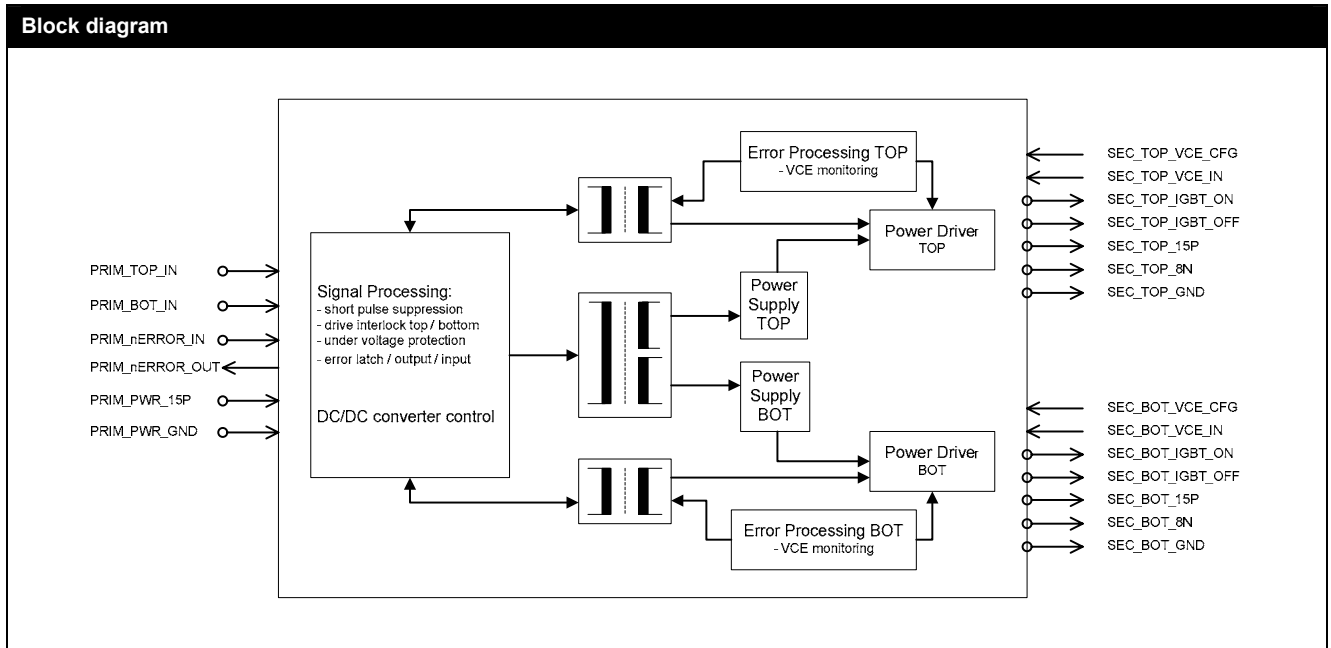
The SKYPER™ 32 core constitutes an interface between IGBT modules and the controller. This core is a half bridge driver. Basic functions for driving, potential separation and protection are integrated in the driver. Thus it can be used to build up a driver solution for IGBT modules.

## Features of SKYPER™ 32

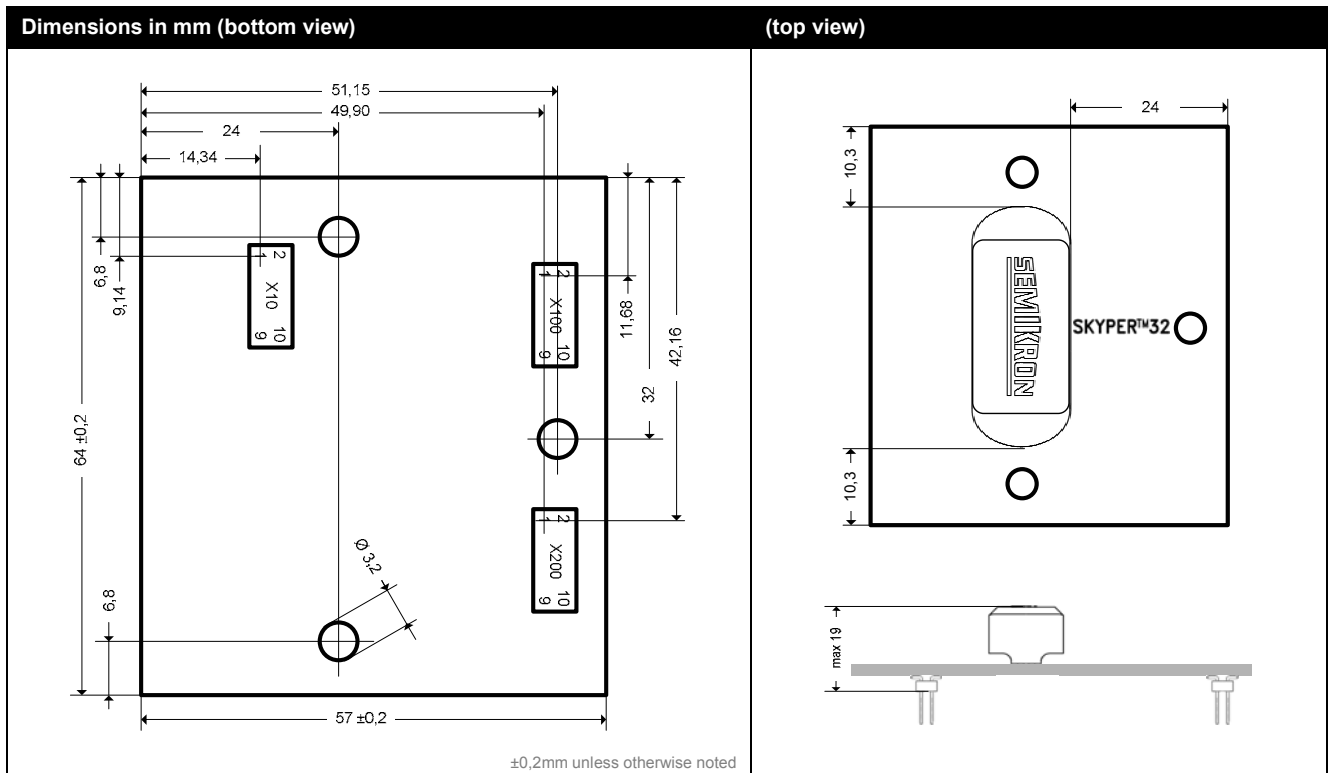
- Two output channels
- Integrated potential free power supply for the secondary side
- Short Pulse Suppression (SPS)
- Under Voltage Protection (UVP)
- Drive interlock (dead time) top / bottom (DT)
- Dynamic Short Circuit Protection (DSCP) by  $V_{CE}$  monitoring and direct switch off
- Shut Down Input (SDI)
- Failure Management
- Expandable by External Boost Capacitors (BC)
- DC bus voltage up to 1200V



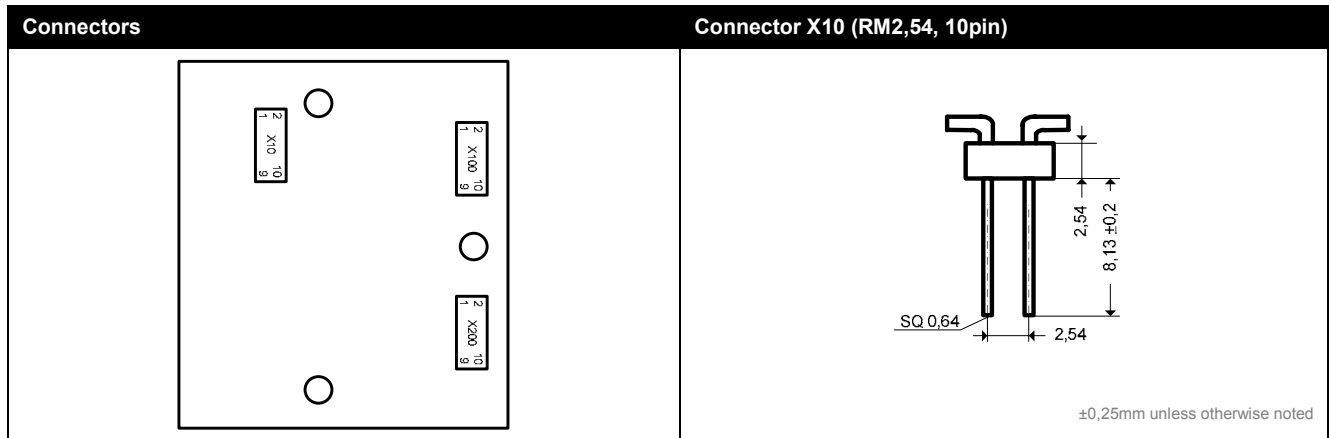
## Block diagram



## Dimensions

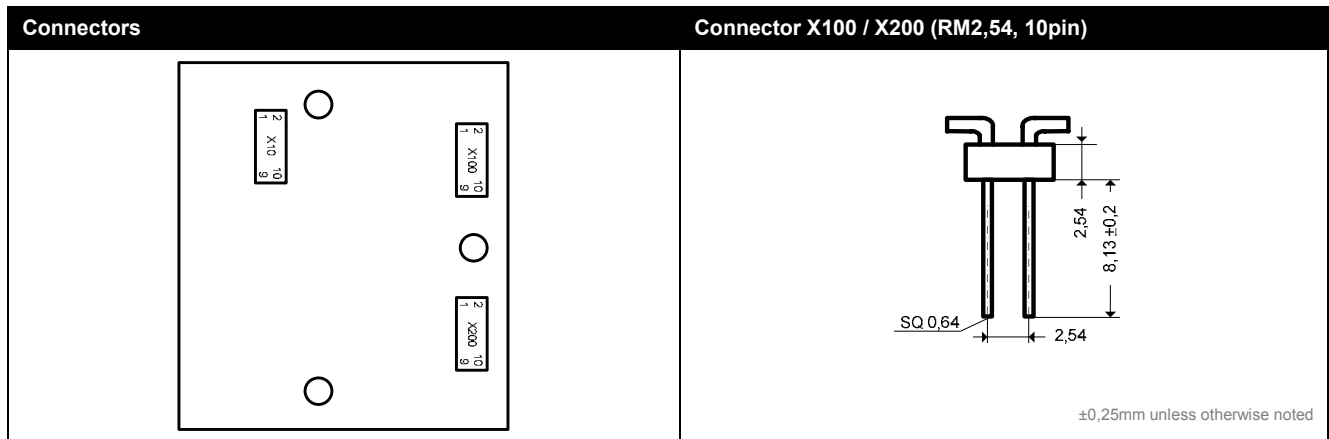


## PIN Array – Primary Side



PIN	Signal	Function	Specification
X10:01	PRIM_PWR_GND	GND for power supply and GND for digital signals	
X10:02	PRIM_PWR_GND	GND for power supply and GND for digital signals	
X10:03	PRIM_nERROR_OUT	ERROR output	LOW = NO ERROR; open collector output; max. 30V / 15mA (external pull up resistor necessary)
X10:04	PRIM_nERROR_IN	ERROR input	5V logic; LOW active
X10:05	PRIM_PWR_GND	GND for power supply and GND for digital signals	
X10:06	PRIM_PWR_GND	GND for power supply and GND for digital signals	
X10:07	PRIM_TOP_IN	Switching signal input (TOP switch)	Digital 15 V; 10 kOhm impedance; LOW = TOP switch off; HIGH = TOP switch on
X10:08	PRIM_BOT_IN	Switching signal input (BOTTOM switch)	Digital 15 V; 10 kOhm impedance; LOW = BOT switch off; HIGH = BOT switch on
X10:09	PRIM_PWR_15P	Drive core power supply	Stabilised +15V ±4%
X10:10	PRIM_PWR_15P	Drive core power supply	Stabilised +15V ±4%

## PIN Array – Secondary Side

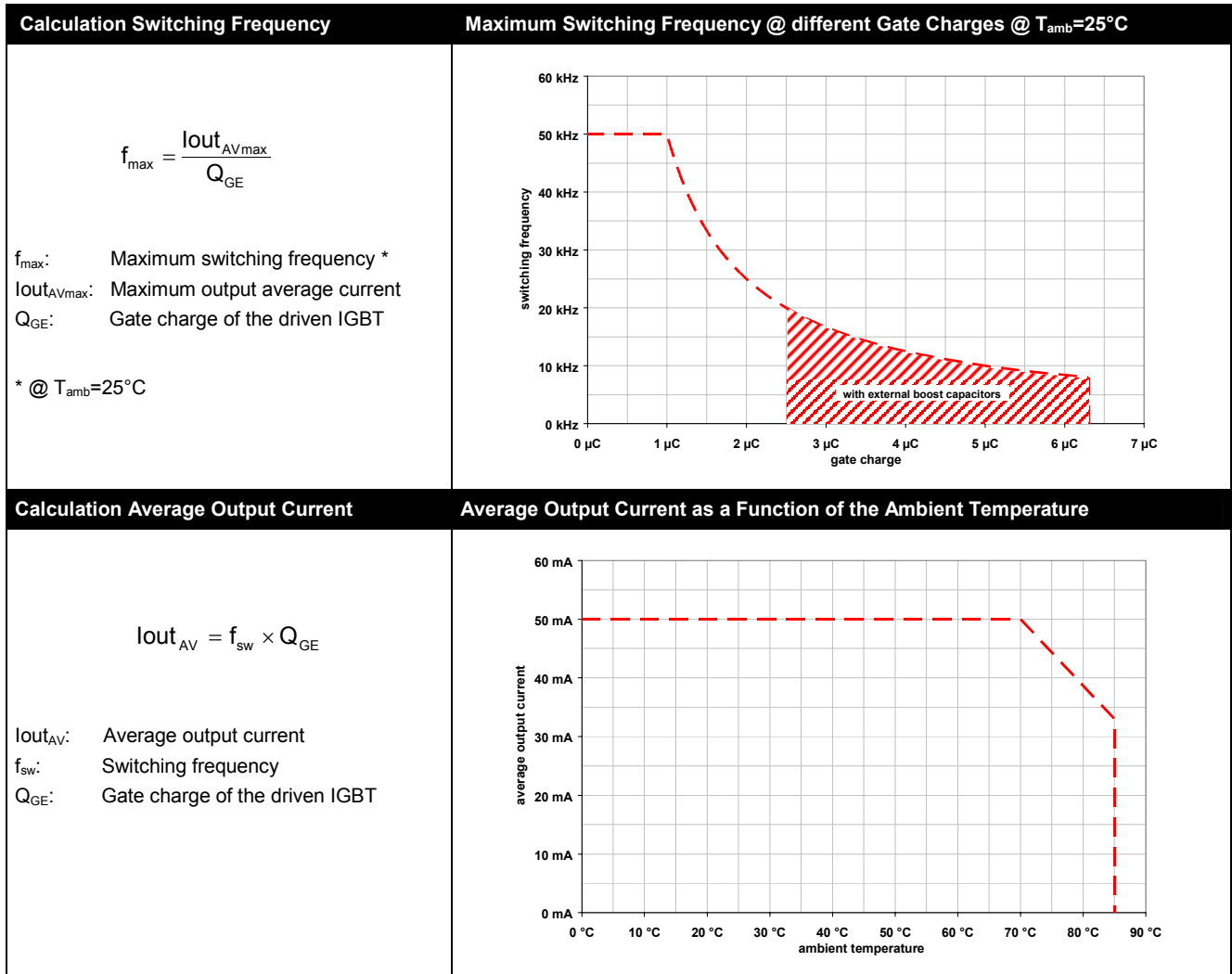


PIN	Signal	Function	Specification
X100:01	SEC_TOP_VCE_CFG	Input reference voltage adjustment	
X100:02	SEC_TOP_VCE_IN	Input $V_{CE}$ monitoring	
X100:03	SEC_TOP_15P	Output power supply for external buffer capacitors	Stabilised +15V
X100:04	SEC_TOP_15P	Output power supply for external buffer capacitors	Stabilised +15V
X100:05	SEC_TOP_GND	GND for power supply and GND for digital signals	
X100:06	SEC_TOP_IGBT_ON	Switch on signal TOP IGBT	
X100:07	SEC_TOP_GND	GND for power supply and GND for digital signals	
X100:08	SEC_TOP_IGBT_OFF	Switch off signal TOP IGBT	
X100:09	SEC_TOP_8N	Output power supply for external buffer capacitors	Stabilised -7V
X100:10	SEC_TOP_8N	Output power supply for external buffer capacitors	Stabilised -7V
X200:01	SEC_BOT_VCE_CFG	Input reference voltage adjustment	
X200:02	SEC_BOT_VCE_IN	Input $V_{CE}$ monitoring	
X200:03	SEC_BOT_15P	Output power supply for external buffer capacitors	Stabilised +15V
X200:04	SEC_BOT_15P	Output power supply for external buffer capacitors	Stabilised +15V
X200:05	SEC_BOT_GND	GND for power supply and GND for digital signals	
X200:06	SEC_BOT_IGBT_ON	Switch on signal BOT IGBT	
X200:07	SEC_BOT_GND	GND for power supply and GND for digital signals	
X200:08	SEC_BOT_IGBT_OFF	Switch off signal BOT IGBT	
X200:09	SEC_BOT_8N	Output power supply for external buffer capacitors	Stabilised -7V
X200:10	SEC_BOT_8N	Output power supply for external buffer capacitors	Stabilised -7V

## Driver Performance

The driver is designed for application with half bridges or single modules and a maximum gate charge per pulse  $< 2,5\mu\text{C}$  ( $< 6,3\mu\text{C}$  with external boost capacitors). The charge necessary to switch the IGBT is mainly depending on the IGBT's chip size, the DC-link voltage and the gate voltage. This correlation is shown in module datasheets. It should, however, be considered that the driver is turned on at +15V and turned off at -7V. Therefore, the gate voltage will change by 22V during each switching procedure. Unfortunately, many datasheets do not show negative gate voltages. In order to determine the required charge, the upper leg of the charge curve may be prolonged to +22V for determination of approximate charge per switch.

The medium output current of the driver is determined by the switching frequency and the gate charge. The maximum switching frequency may be calculated with the shown equation and is limited by the average current of the driver power supply and the power dissipation of driver components.



**Please note:**

The maximum value of the switching frequency is limited to 50kHz due to switching reasons.

## Insulation

Magnetic transformers are used for insulation between gate driver primary and secondary side. The transformer set consists of pulse transformers which are used bidirectional for turn-on and turn-off signals of the IGBT and the error feedback between secondary and primary side, and a DC/DC converter. This converter provides a potential separation (galvanic separation) and power supply for the two secondary (TOP and BOT) sides of the driver. Thus, external transformers for external power supply are not required.

### Creepage and Clearance Distance in mm

Primary to secondary	Min. 12,2
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## Isolation Test Voltage

The isolation test voltage represents a measure of immunity to transient voltages. The maximum test voltage and time applied once between input and output, and once between output 1 and output 2 are indicated in the absolute maximum ratings. The high-voltage isolation tests and repeated tests of an isolation barrier can degrade isolation capability due to partial discharge. Repeated isolation voltage tests should be performed with reduced voltage. The test voltage must be reduced by 20% for each repeated test.

The isolation of the isolation barrier (transformer) is checked in the part. With exception of the isolation barrier, no active parts, which could break through are used. An isolation test is not performed as a series test. Therefore, the user can perform once the isolation test with voltage and time indicated in the absolute maximum ratings.

**Please note:**

An isolation test is not performed at SEMIKRON as a series test.

## Auxiliary Power Supply

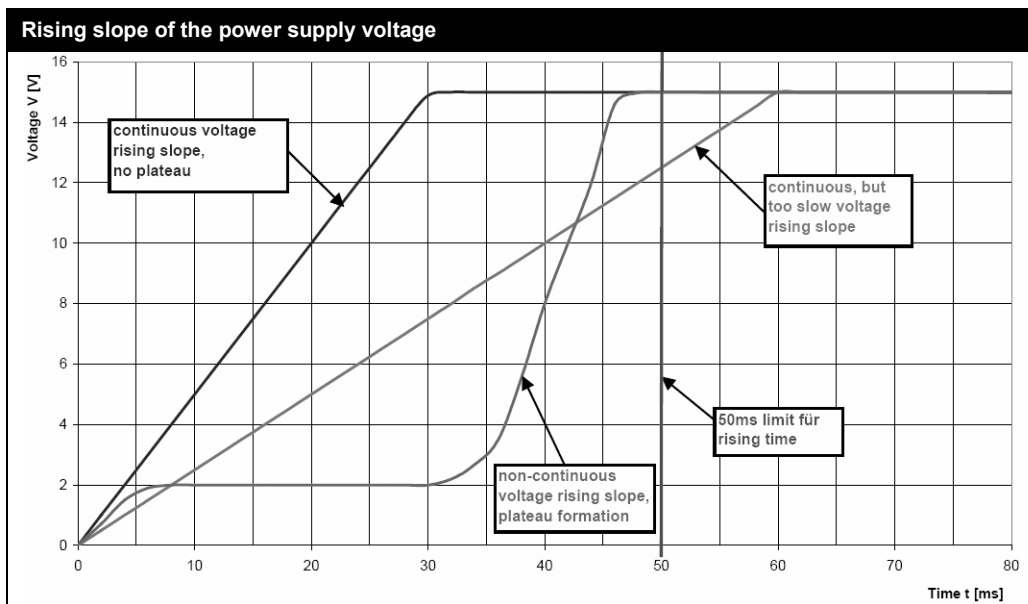
A few basic rules should be followed when dimensioning the customer side power supply for the driver. The following table shows the required features of an appropriate power supply.

Requirements of the auxiliary power supply	
Regulated power supply	+15V ±4%
Maximum rise time of auxiliary power supply	50ms
Minimum peak current of auxiliary supply	1A
Power on reset completed after	150ms

**Please note:**

Do not apply switching signals during power on reset.

The supplying switched mode power supply may not be turned-off for a short time as consequence of its current limitation. Its output characteristic needs to be considered. Switched mode power supplies with fold-back characteristic or hiccup-mode can create problems if no sufficient over current margin is available. The voltage has to rise continuously and without any plateau formation as shown in the following diagram.



If the power supply is able to provide a higher current, a peak current will flow in the first instant to charge up the input capacitances on the driver. Its peak current value will be limited by the power supply and the effective impedances (e.g. distribution lines), only.

It is recommended to avoid the paralleling of several customer side power supply units. Their different set current limitations may lead to dips in the supply voltage.

The driver is ready for operation typically 150ms after turning on the supply voltage. The driver error signal PRIM\_nERROR\_OUT is operational after this time. Without any error present, the error signal will be reset.

To assure a high level of system safety the TOP and BOT signal inputs should stay in a defined state (OFF state, LOW) during driver turn-on time. Only after the end of the power-on-reset, IGBT switching operation shall be permitted.



## Under Voltage Protection of driver power supply (UVP)

The internally detected supply voltage of the driver has an under voltage protection. The table below gives an overview of the trip level.

Supply voltage	UVP level
Regulated +15V ±4%	13,5V

If the internally detected supply voltage of the driver falls below this level, the IGBTs will be switched off (IGBT driving signals set to LOW). The input side switching signals of the driver will be ignored. The error memory will be set, and the output PRIM\_nERROR\_OUT changes to the HIGH state.

## Input Signals

The signal transfer to each IGBT is made with pulse transformers, used for switching on and switching off of the IGBT. The inputs have a Schmitt Trigger characteristic and a positive / active high logic (input HIGH = IGBT on; input LOW = IGBT off). It is mandatory to use circuits which switch active to +15V and 0V. Pull up and open collector output stages must not be used for TOP / BOT control signals. It is recommended choosing the line drivers according to the demanded length of the signal lines.

**Please note:**

It is not permitted to apply switching pulses shorter than 1µs.

**TOP / BOT Input**

**User Side**

PRIM\_TOP\_IN — INPUT TOP

PRIM\_BOT\_IN — INPUT BOT

PRIM\_PWR\_GND — GND

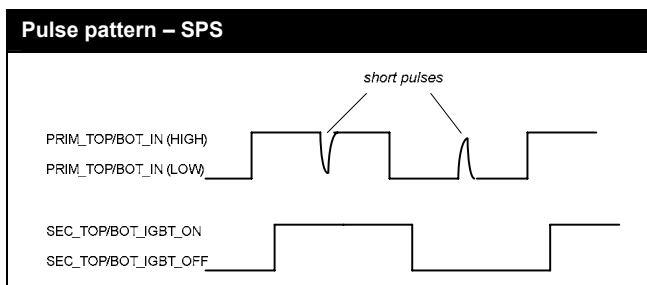
PRIM\_PWR\_GND — GND

C 1nF    C 1nF

A capacitor is connected to the input to obtain high noise immunity. This capacitor can cause for current limited line drivers a little delay of few ns, which can be neglected. The capacitors have to be placed as close as possible to the driver interface.

## Short Pulse Suppression (SPS)

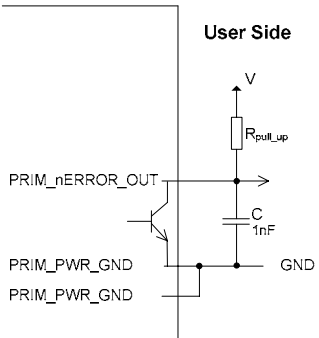
This circuit suppresses short turn-on and off-pulses of incoming signals. This way the IGBTs are protected against spurious noise as they can occur due to bursts on the signal lines. Pulses shorter than 625ns are suppressed and all pulses longer than 750ns get through for 100% probability. Pulses with a length in-between 625ns and 750ns can be either suppressed or get through.



## Failure Management

Any error detected will set the error latch and force the output PRIM\_nERROR\_OUT into HIGH state. Switching pulses from the controller will be ignored. Connected and switched off IGBTs remain turned off. The switched off IGBTs remain turned off. A reset of the latched error memory is only possible if no failure is present anymore and if the TOP and BOT input signals are set to the LOW level for a period of  $t_{pERRRESET} > 9\mu s$ .

The output PRIM\_nERROR\_OUT is an open collector output. For the error evaluation an external pull-up-resistor is necessary pulled-up to the positive operation voltage of the control logic (LOW signal = no error present, wire break safety is assured).

Open collector error transistor	Application hints
	<p>An external resistor to the controller logic high level is required. The resistor has to be in the range of <math>V / I_{max} &lt; R_{pull\_up} &lt; 10k\Omega</math>.                      PRIM_nERROR_OUT can operate to maximum 30V and can switch a maximum of 15mA.</p> <p><b>Example:</b>                      For <math>V = +15V</math> the needed resistor should be in the range <math>R_{pull\_up} = (15V/15mA) \dots 10k\Omega \Rightarrow 1k\Omega \dots 10k\Omega</math>.</p>

**Please note:**

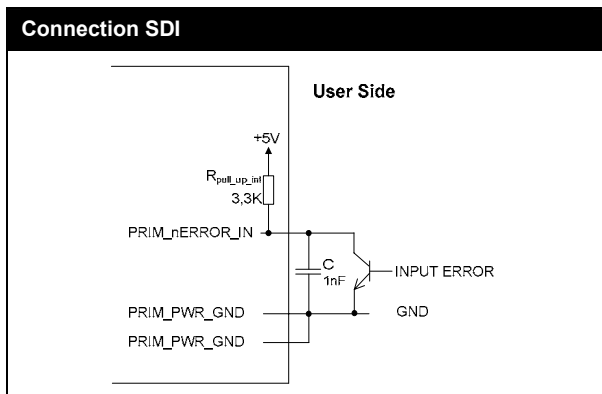
The error output PRIM\_ERROR\_OUT is not short circuit proof.

## Shut Down Input (SDI)

The shut down input / error input signal can gather error signals of other hardware components for switching off the IGBT (input HIGH = no turn-off; input LOW = turn-off).

A LOW signal at PRIM\_nERROR\_IN will set the error latch and force the output PRIM\_nERROR\_OUT into HIGH state. Switching pulses from the controller will be ignored. A reset of the latched error memory is only possible if no LOW signal at PRIM\_nERROR\_IN is present anymore and if the TOP and BOT input signals are set to the LOW level for a period of  $t_{pERRRESET} > 9\mu s$ .

The SDI function can be disabled by no connection or connecting to 5V.



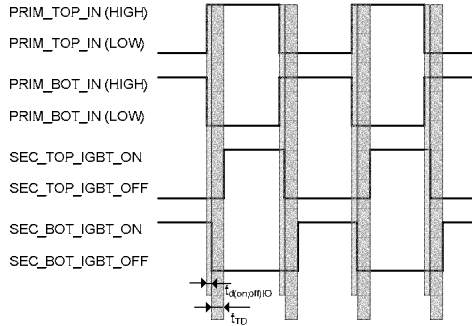
## Dead Time generation (Interlock TOP / BOT) (DT)

The DT circuit prevents, that TOP and BOT IGBT of one half bridge are switched on at the same time (shoot through). The dead time is not added to a dead time given by the controller. Thus the total dead time is the maximum of "built in dead time" and "controller dead time". It is possible to control the driver with one switching signal and its inverted signal.

**Please note:**

The generated dead time is fixed and cannot be changed.

### Pulse pattern – DT



- The total propagation delay of the driver is the sum of interlock dead time ( $t_{DT}$ ) and driver input output signal propagation delay ( $t_{d(on;off)O}$ ) as shown in the pulse pattern. Moreover the switching time of the IGBT chip has to be taken into account (not shown in the pulse pattern).
- In case both channel inputs (PRIM\_TOP\_IN and PRIM\_BOT\_IN) are at high level, the IGBTs will be turned off.
- If only one channel is switching, there will be no interlock dead time.

**Please note:**

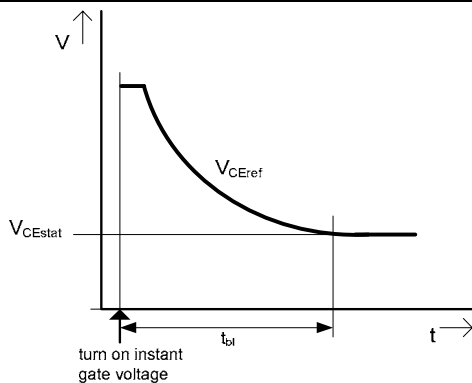
No error message will be generated when overlap of switching signals occurs.

## Dynamic Short Circuit Protection by $V_{CEsat}$ monitoring / de-saturation monitoring (DSCP)

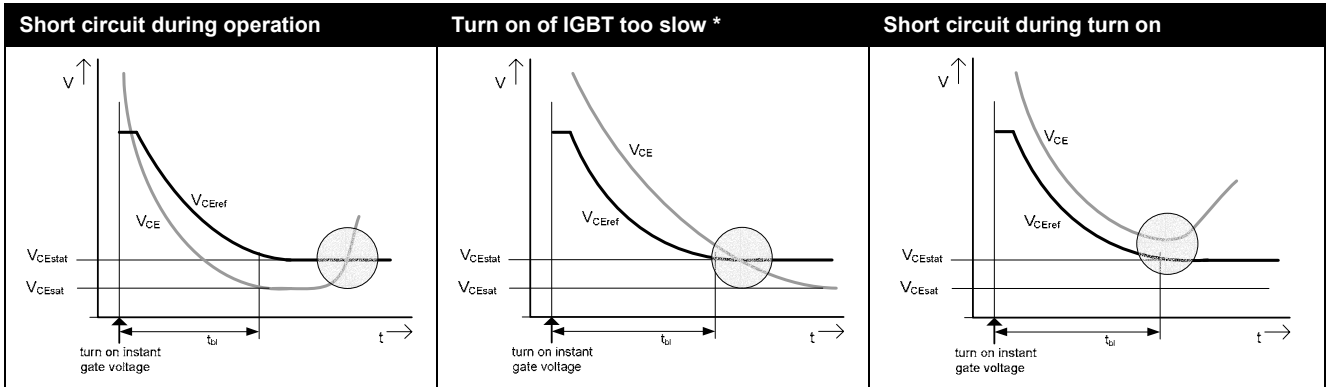
The DSCP circuit is responsible for short circuit sensing. It monitors the collector-emitter voltage  $V_{CE}$  of the IGBT during its on-state. Due to the direct measurement of  $V_{CEsat}$  on the IGBT's collector, the DSCP circuit switches off the IGBTs and an error is indicated.

The reference voltage  $V_{CEref}$  may dynamically be adapted to the IGBTs switching behaviour. Immediately after turn-on of the IGBT, a higher value is effective than in steady state. This value will, however, be reset, when the IGBT is turned off.  $V_{CEstat}$  is the steady-state value of  $V_{CEref}$  and is adjusted to the required maximum value for each IGBT by an external resistor  $R_{CE}$ . It may not exceed 10V. The time constant for the delay (exponential shape) of  $V_{CEref}$  may be controlled by an external capacitor  $C_{CE}$ , which is connected in parallel to  $R_{CE}$ . It controls the blanking time  $t_{bl}$  which passes after turn-on of the IGBT before the  $V_{CEsat}$  monitoring is activated. This makes an adaptation to any IGBT switching behaviour possible.

### Reference Voltage ( $V_{CEref}$ ) Characteristic



After  $t_{bl}$  has passed, the  $V_{CE}$  monitoring will be triggered as soon as  $V_{CEsat} > V_{CEref}$  and will turn off the IGBT. The error memory will be set, and the output PRIM\_nERROR\_OUT changes to the HIGH state. Possible failure modes are shown in the following pictures.



\* or adjusted blanking time too short

## Adjustment of DSCP

The external components  $R_{CE}$  and  $C_{CE}$  are applied for adjusting the steady-state threshold the blanking time.

Connection $R_{CE}$ and $C_{CE}$	Dimensioning of $R_{CE}$ and $C_{CE}$
	$R_{CE} [k\Omega] = -17k\Omega \cdot \ln \left( 1 - \frac{V_{CEstat} + R_{VCE} \cdot \frac{V}{k\Omega}}{8,5V} \right)$ $C_{CE} [pF] = \frac{t_{bl} [\mu s] - 2,5\mu s - 0,11 \frac{\mu s}{\Omega} \cdot R_{CE}}{0,00323 \frac{\mu s}{pF}}$ <p> <math>V_{CEstat}</math>: Collector-emitter threshold static monitoring voltage  <math>t_{blx}</math>: Blanking time                 </p> <p> <math>V_{CEstat\_max} = 8V</math> (<math>R_{VCE} = 0\Omega</math>)  <math>V_{CEstat\_max} = 7V</math> (<math>R_{VCE} = 1k\Omega</math>)                 </p> <p><b>Please Note:</b>                      The equations are calculated considering the use of high voltage diode BY203/20S. The calculated values <math>V_{CEstat}</math> and <math>t_{bl}</math> are typical values at room temperature. These values can and do vary in the application (e.g. tolerances of used high voltage diode, resistor <math>R_{CE}</math>, capacitor <math>C_{CE}</math>).                      The DSCP function is not recommended for over current protection.</p>

## Application hints

If the DSCP function is not used, for example during the experimental phase, SEC\_TOP\_VCE\_IN must be connected with SEC\_TOP\_GND for disabling SCP @ TOP side and SEC\_BOT\_VCE\_IN must be connected with SEC\_BOT\_GND for disabling SCP @ BOT side.

## High Voltage Diode for DSCP

The high voltage diode blocks the high voltage during IGBT off state. The connection of this diode between driver and IGBT is shown in the following schematic.

Connection High Voltage Diode	Characteristics
<p>The diagram shows two IGBTs, labeled TOP and BOT, connected to a common Load. Each IGBT has its emitter connected to a common ground (SEC_TOP_GND for TOP, SEC_BOT_GND for BOT). A high-voltage diode (BY203/20S) is connected in series between the collector of each IGBT and the Load. A resistor <math>R_{VCE}</math> is connected in series with the diode. The IGBTs are also connected to a driver through gate resistors <math>R_{GE}</math> and collector-emitter capacitors <math>C_{CE}</math>. The driver terminals are labeled SEC_TOP_VCE_IN, SEC_TOP_VCE_CFG, SEC_BOT_VCE_IN, and SEC_BOT_VCE_CFG.</p>	<ul style="list-style-type: none"> <li>Reverse blocking voltage of the diode shall be higher than the used IGBT.</li> <li>Reverse recovery time of the fast diode shall be lower than <math>V_{CE}</math> rising of the used IGBT.</li> <li>Forward voltage of the diode: 1,5V @ 2mA forward current (<math>T_j=25^\circ\text{C}</math>).</li> </ul> <p><b>A collector series resistance <math>R_{VCE}</math> (1k<math>\Omega</math> / 0,4W) must be connected for 1700V IGBT operation.</b></p>

## Gate resistors

The output transistors of the driver are MOSFETs. The sources of the MOSFETs are separately connected to external terminals in order to provide setting of the turn-on and turn-off speed of each IGBT by the external resistors  $R_{Gon}$  and  $R_{Goff}$ . As an IGBT has input capacitance (varying during switching time) which must be charged and discharged, both resistors will dictate what time must be taken to do this. The final value of the resistance is difficult to predict, because it depends on many parameters as DC link voltage, stray inductance of the circuit, switching frequency and type of IGBT.

Connection $R_{Gon}$ , $R_{Goff}$	Application Hints
<p>The diagram shows two IGBTs, labeled TOP and BOT, connected to a common Load. Each IGBT has its emitter connected to a common ground (SEC_TOP_GND for TOP, SEC_BOT_GND for BOT). A gate resistor <math>R_{Gon}</math> is connected between the driver terminal SEC_TOP_IGBT_ON (or SEC_BOT_IGBT_ON) and the gate of the IGBT. A gate resistor <math>R_{Goff}</math> is connected between the driver terminal SEC_TOP_IGBT_OFF (or SEC_BOT_IGBT_OFF) and the gate of the IGBT. The IGBTs are also connected to a driver through gate resistors <math>R_{GE}</math> and collector-emitter capacitors <math>C_{CE}</math>. The driver terminals are labeled SEC_TOP_IGBT_ON, SEC_TOP_IGBT_OFF, SEC_BOT_IGBT_ON, and SEC_BOT_IGBT_OFF.</p>	<p>The gate resistor influences the switching time, switching losses, <math>dv/dt</math> behaviour, etc. and has to be selected very carefully. Due to this influence a general value for the gate resistors cannot be recommended. The gate resistor has to be optimized according to switching behaviour and over voltage peaks within the specific circuitry.</p> <p>By increasing <math>R_{Gon}</math> the turn-on speed will decrease. The reverse peak current of the free-wheeling diode will diminish.</p> <p>By increasing <math>R_{Goff}</math> the turn-off speed of the IGBT will decrease. The inductive peak over voltage during turn-off will diminish.</p> <p>In order to ensure locking of the IGBT even when the driver supply voltage is turned off, a resistance (<math>R_{GE}</math>) has to be integrated.</p>

### Please note:

Do not connect the terminals SEC\_TOP\_IGBT\_ON with SEC\_TOP\_IGBT\_OFF and SEC\_BOT\_IGBT\_ON with SEC\_BOT\_IGBT\_OFF, respectively.

## External Boost Capacitors (BC)

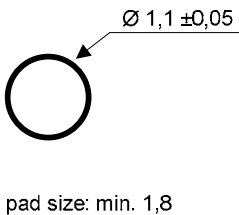
The rated gate charge of the driver may be increase by additional boost capacitors to drive IGBT with large gate capacitance.

Connection External Boost Capacitors	Dimensioning of $C_{boost}$
	<ul style="list-style-type: none"> <li>▪ <math>C_{boost15P} [\mu F] = Q_{GE} [\mu C] \times 1/V - 2,2\mu F</math></li> <li>▪ <math>C_{boost8N} [\mu F] = Q_{GE} [\mu C] \times 2/V - 4,7\mu F</math></li> <li>▪ <math>Q_{GE}</math>: Gate charge of the IGBT @ <math>V_{GE} = -7 \dots +15V</math></li> <li>▪ Minimum rated voltage <math>C_{boost15P}</math>: 25V</li> <li>▪ Minimum rated voltage <math>C_{boost8N}</math>: 16V</li> <li>▪ Type of capacitor: ceramic capacitor</li> </ul> <p><b>Please consider the maximum rating four output charge per pulse of the gate driver.</b></p>
<b>Application Hints</b>	
<p>The external boost capacitors should be connected as close as possible to the gate driver and to have low inductance.</p>	

## Application Example

Connection Schematic	
	<ul style="list-style-type: none"> <li>- application example for 1200V IGBT</li> <li>- <math>Q_{out/pulse} = 5\mu C</math></li> <li>- <math>V_{CRef} = 5,5V</math></li> <li>- <math>t_{bl} = 5,5\mu s</math></li> </ul>

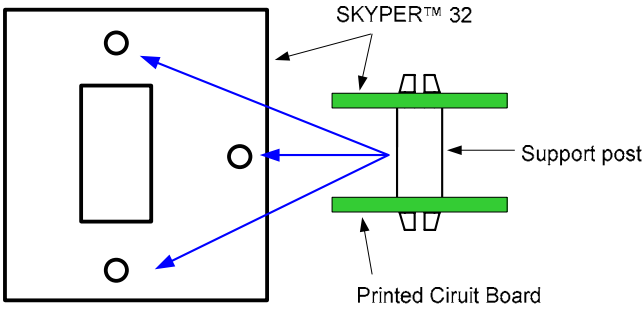
## Mounting Notes

Soldering Hints	Drill Hole & Pad Size in mm
<p>The temperature of the solder must not exceed 260°C, and solder time must not exceed 10 seconds.</p> <p>The ambient temperature must not exceed the specified maximum storage temperature of the driver.</p> <p>The solder joints should be in accordance to IPC A 610 Revision D (or later) - Class 3 (Acceptability of Electronic Assemblies) to ensure an optimal connection between driver core and printed circuit board.</p>	 <p>pad size: min. 1,8</p>

**Please note:**

The driver is not suited for hot air reflow or infrared reflow processes.

The connection between driver core and printed circuit board should be mechanical reinforced by using support posts.

Use of Support Posts	
	<p>Product information of suitable support posts and distributor contact information is available at e.g. <a href="http://www.richco-inc.com">http://www.richco-inc.com</a> (e.g. series DLMSPM, LCBST).</p>

**Please note:**

The use of aggressive materials in cleaning and potting process of driver core may be detrimental for the device parameters. If the driver core is coated by the user, any warranty (Gewährleistung) expires.

## Environmental Conditions

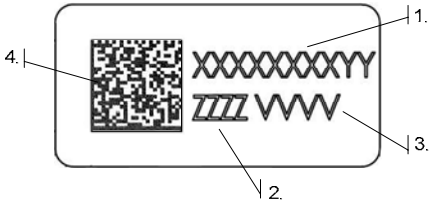
The driver core is type tested under the environmental conditions below.

Conditions	Values (max.)
Vibration	Sinusoidal sweep 20Hz ... 500Hz, 5g, 26 sweeps per axis (x, y, z) - Tested acc. IEC 68-2-6 - Connection between driver core and printed circuit board mechanical reinforced by using support posts.
Shock	Half-sinusoidal pulse, 5g, shock width 18ms, 3 shocks in each direction ( $\pm x$ , $\pm y$ , $\pm z$ ), 18 shocks in total - Tested acc. IEC 68-2-27 - Connection between driver core and printed circuit board mechanical reinforced by using support posts.

The characteristics and further environmental conditions are indicated in the data sheet.

## Marking

Every driver core is marked. The marking contains the following items.

Part Marking Information											
 <p>1. SEMIKRON part number (8 digits) + version number (2 digits)                  2. Date code (4 digits): YYWW                  3. Continuous number referred to date code (4 digits)                  4. Data matrix code</p>	<p>The Data Matrix Code is described as follows:</p> <ul style="list-style-type: none"> <li>▪ Type: EEC 200</li> <li>▪ Standard: ICO / IEC 16022</li> <li>▪ Cell size: 0,254 - 0,3 mm</li> <li>▪ Dimension: 5 × 5 mm</li> <li>▪ The following data is coded:</li> </ul> <table style="margin-left: 40px;"> <tr> <td style="text-align: center;">❶</td> <td style="text-align: center;">❷</td> <td style="text-align: center;">❸</td> <td style="text-align: center;">❹</td> <td style="text-align: center;">❺</td> </tr> <tr> <td style="text-align: center;">XXXXXXXXXY</td> <td style="text-align: center;">ZZZ</td> <td style="text-align: center;">VVV</td> <td></td> <td></td> </tr> </table> <ul style="list-style-type: none"> <li>❶ 8 digits part number 2 digits version number</li> <li>❷ 1 digit blank</li> <li>❸ 4 digits date code</li> <li>❹ 1 digit blank</li> <li>❺ 4 digits continuous number</li> </ul>	❶	❷	❸	❹	❺	XXXXXXXXXY	ZZZ	VVV		
❶	❷	❸	❹	❺							
XXXXXXXXXY	ZZZ	VVV									

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